1. A method comprising:

reading a second memory portion that stores a specific physical address corresponding to an input virtual address before internally stored data accessed from a first memory portion based on the input virtual address entirely matches the input virtual address.

2. The method of claim 1, including using at least two register files, one for said first memory portion and the other for said second memory portion.

3. The method of claim 2, including decoding the input virtual address before accessing said at least two register files, wherein said at least two register files having a multiplicity of write and read ports that enable and simultaneously accessing to the internally stored data and said specific physical address output.

4. The method of claim 1, wherein matching includes:

storing a multiplicity of tags in the internally stored data;

receiving indexing data within the input virtual address;

examining said indexing data to identify corresponding at least two tags from the internally stored data;

comparing said indexing data with said at least two tags; and

after any one of the tags of said at least two tags in the internally stored data matches said indexing data, signaling an enable signal to output the specific physical address output.

5. The method of claim 2, including:

storing an identifying data value in said one of said at least two register files for the specific physical address output; and

storing a specific data associated with the identifying data value for the specific physical address output in the other register file of said at least two register files.

6. The method of claim 5, including accessing the second memory portion for the specific data before a match occurs between the identifying data value and the specific data.

7. A method comprising:

reading a physical address value corresponding to a virtual address that includes an input data word for address translation of said virtual address into a specific data address; and

comparing the input data word to internally stored data in parallel with said reading.

8. The method of claim 7, including:

selecting a page size for the virtual address;

varying the number and position of compared bits for the virtual address based on the selected page size; and

if any one of the internally stored data matches the input data word, signaling an enable signal to output the specific data address.

9. The method of claim 8, including defining a set associativity for a multiplicity of virtual memory locations that hold the internally stored data and translating the virtual address using any one of the multiplicity of virtual memory locations based on the set associativity.

10. The method of claim 9, including storing the internally stored data in a first register file adapted to fire simultaneously with a second register file and decoding selected bits of the virtual address before accessing said first and second register files wherein the selected bits are indicative of a bank page size.

11. A content addressed buffer comprising:

a data bank including a first memory portion to store internally stored data selectively accessible based on an input virtual address and a second memory portion accessible in parallel to said first memory portion to translate the input virtual address into a specific physical address before the internally stored data entirely matches the input virtual address.

12. The content addressed buffer of claim 11, including a multiplexer to select the specific physical address output from said data bank.

13. The content addressed buffer of claim 12, said first memory portion is a virtual address register file, and said second memory portion is a physical address register file, wherein each of said virtual and physical address register files having a multiplicity of write and read ports.

14. The content addressed buffer of claim 13, further including a selector to select the number and position of compared bits for the input virtual address based on the page size selected, wherein said virtual address register file to store a multiplicity of tags in the internally stored data and said physical address register file to store the specific physical address output.

15. The content addressed buffer of claim 14, wherein said data bank including:

an address selector to receive indexing data within the input virtual address to examine said indexing data and to identify corresponding at least two tags from the internally stored data;

a decoder, coupled to said address selector, to decode the input virtual address before accessing said virtual and physical address register files to enable simultaneous access to the internally stored data and said specific physical address output, respectively; and

a comparator, coupled to said decoder, to compare said indexing data with said at least two tags and after any one of the tags of said at least two tags in the internally stored data matches said indexing data, signaling an enable signal to said multiplexer to output the specific physical address output.

16. A system comprising:

a processor having a content addressed buffer with a data bank including a first memory portion storing internally stored data accessible selectively based on an input virtual address and a second memory portion accessible in parallel to said first memory portion for translation of the input virtual address into a specific physical address before the internally stored data entirely matches the input virtual address and the internally stored data; and

a flash memory coupled to said processor.

17. The system of claim 16, wherein said content addressed buffer is a set associative translation look aside buffer.

18. The system of claim 16, said first memory portion is a virtual address register file, and said second memory portion is a physical address register file, wherein each of said virtual and physical address register files having a multiplicity of write and read ports.

19. The system of claim 16, said first memory portion is a first static random access memory that stores a virtual address, and said second memory portion is a second static random access memory that stores a physical address.

20. The system of claim 19, said content addressed buffer further includes a selector to select a page size for the input virtual address and a register to select the number and position of compared bits for the input virtual address based on the selected page size.

21. A processor comprising:

a content addressed buffer with a data bank including a first memory portion storing internally stored data selectively accessible based on an input virtual address and a second memory portion accessible in parallel to said first memory portion for translation of the input virtual address into a specific physical address before the internally stored data entirely matches the input virtual address.

22. The processor of claim 21, wherein said content addressed buffer is a set associative translation look aside buffer.

23. The processor of claim 21, said first memory portion is a virtual address register file, and said second memory portion is a physical address register file, wherein each of said virtual and physical address register files having a multiplicity of write and read ports.

24. The processor of claim 21, said first memory portion is a first static random access memory that stores a virtual address, and said second memory portion is a second static random access memory that stores a physical address.

25. The processor of claim 24, said content addressed buffer further includes a selector to select a page size for the input virtual address and a register to select the number and position of compared bits for the input virtual address based on the selected page size.